WHAT IS CLAIMED IS:

Sub a1

1. A display device comprising:

a pixel portion in which (m x 2n) pixels, each including at least one TFT, are arranged in matrix form (both m and n are natural numbers);

a source driver for supplying video signals to 2n source signal lines S1, S2, ···· , Sn, Sn+1, Sn+2, ···· , S2n;

a first gate driver for supplying selection signals to m first gate signal lines G1L, G2L, ···· , GmL; and

a second gate driver for supplying selection signals to m second gate signal lines G1R, G2R, ···· , GmR, wherein:

the pixels connected to the source signal lines S1, S2, ···· , Sn are supplied with the selection signals from the first gate signal lines G1L, G2L, ···· , GmL;

the pixels connected to the source signal lines Sn+1, SN+2, ···· , S2n are supplied with the selection signals from the second gate signal lines G1R, G2R, ···· , GmR;

the selection signal starts to be supplied to the second gate signal line G1R while the selection signal is supplied to the first gate signal line G1L; and

the selection signal starts to be supplied to the first gate signal line G1L while the selection signal is supplied to the second gate signal line G1R.

Sub a2

2. A display device comprising:

a pixel portion in which (m x 2n) pixels, each including at least one TFT, are arranged in matrix form (both m and n are natural numbers);

a source driver for supplying video signals to 2n source signal lines S1, S2, ···· , Sn, Sn+1, Sn+2, ···· , S2n;

a first gate driver for supplying selection signals to m first gate signal lines G1L, G2L, ···· , GmL; and

a second gate driver for supplying selection signals to m second gate signal lines G1R, G2R, ···· , GmR, wherein:

the pixels connected to the source signal lines S1, S2, ···· , Sn are supplied with the selection signals from the first gate signal lines G1L, G2L, ···· , GmL;

the pixels connected to the source signal lines Sn+1, Sn+2, ···· , S2n are supplied with the selection signals from the second gate signal lines G1R, G2R, ···· , GmR; and

the selection signals are sequentially supplied to the first gate signal line G1L, the second gate signal line G1R, the first gate signal line G2L, the second gate signal line G2R, ···· , the first gate signal line GmL, and the second gate signal line GmR in this order with a delay of a half period between the respective adjacent gate signal lines.

Sub D'

3. A rear projector comprising three display devices according to claim 1.

4. A rear projector comprising three display devices according to claim 2.

5. A front projector comprising three display devices according to claim 1.

6. A front projector comprising three display devices according to claim 2.

7. A rear projector comprising one display device according to claim 1.

8. A rear projector comprising one display device according to claim 2.

9. A front projector comprising one display device according to claim 1.

10. A front projector comprising one display device according to claim 2.

11. A head mount display comprising a display device according to claim 1.

12. A head mount display comprising a display device according to claim 2.

13. A Computer comprising a display device according to claim 1.

14. A Computer comprising a display device according to claim 2.

15. A video camera comprising a display device according to claim 1.

16. A video camera comprising a display device according to claim 2.

17. A DVD player comprising a display device according to claim 1.

18. A DVD player comprising a display device according to claim 2.

19. A display device comprising a display device according to claim 1.

20. A display device comprising a display device according to claim 2.

21. A display device according to claim 1 is a liquid crystal display device.

22. A display device according to claim 2 is a liquid crystal display device.

Sub C3

23. A method of driving an active matrix display device comprising:

a pixel portion in which (m x 2n) pixels, each including at least one TFT, are arranged in matrix form (both m and n are natural numbers);

a source driver for supplying video signals to 2n source signal lines S1, S2, ···· , Sn, Sn+1, Sn+2, ···· , S2n;

a first gate driver for supplying selection signals to m first gate signal lines G1L, G2L, ···· , GmL; and

a second gate driver for supplying selection signals to m second gate signal lines G1R, G2R, ···· , GmR, wherein said method comprises the steps of:

supplying the pixels connected to the source signal lines S1, S2, ····, Sn with the selection signals from the first gate signal lines G1L, G2L, ····, GmL;

supplying the pixels connected to the source signal lines Sn+1, Sn+2, ····, S2n with the selection signals from the second gate signal lines G1R, G2R, ····, GmR;

starting to supply the selection signal to the second gate signal line G1R while the selection signal is supplied to the first gate signal line G1L; and

starting to supply the selection signal to the first gate signal line G1L while the section signal is supplied to the second gate signal line G1R.

Sub C3

24. A method of driving an active matrix display device comprising:

a pixel portion in which (m x 2n) pixels, each including at least one TFT, are arranged in matrix form (both m and n are natural numbers);

a source driver for supplying video signals to 2n source signal lines S1, S2, ···· , Sn, Sn+1, Sn+2, ···· , S2n;

a first gate driver for supplying selection signals to m first gate signal lines G1L, G2L, ···· , GmL; and

a second gate driver for supplying selection signals to m second gate signal lines G1R, G2R, ···· , GmR, wherein said method comprises the steps of:

supplying the pixels connected to the source signal lines S1, S2, ····, Sn with the selection signals from the first gate lines G1L, G2L, ····, GmL;

supplying the pixels connected to the source signal lines Sn+1, Sn+2, ····, S2n with the selection signals from the second gate lines G1R, G2R, ····, GmR;

starting to supply the selection signal to the second gate signal line G1R while the selection signal is supplied to the first gate signal line G1L; and

starting to supply the selection signal to the first gate signal line G1L while the selection signal is supplied to the second gate signal line G1R.

add a3